REMARKS

Applicant changed the status identifiers of claims 21 and 22 to indicate that those claims have been previously presented. The status identifiers of those claims erroneously indicated in the September 11, 2006, Amendment in Reply to Final Action July 10, 2006, that the claims were "New" even though the claims were first introduced in the Amendment in Reply to Action of February 8, 2006. For the examiner's convenience, applicant presents herein the claim amendments and remarks that were presented in the Amendment in Reply to Final Action July 10, 2006, filed on September 11, 2006.

Applicant amended independent claim 1 to add a feature, similar to the feature previously recited in claim 4, that the state upon which a branch condition is evaluated is made available to a plurality of microengines. Applicant similarly amended independent claims 10, 16 and 19. Applicant further amended claim 1 to recite features similar to those recited in independent claim 16, namely, that each microengine has control logic and execution box that include an arithmetic logic unit and a register set. Further support for the feature pertaining to the microengine is found, for example, in FIG. 3, and in at page 5, line 1 to page 6, line 18 of the originally filed application. Applicant similarly amended independent claims 10 and 19. Additionally, applicant amended claims 11 and 12 to correct antecedent problems, and to make the language recited in claims 11 and 12 consistent with the language recited in independent claim 10. Claim 17 was amended to make the language recited therein consistent with the language recited in independent claim 16. Also, applicant canceled claim 4. After these amendments, claims 1-3, 5 and 7-22 are pending in the above-identified patent application. Claims 1, 10, 16 and 19 are independent claims.

The examiner rejected claims 1 and 19 under 35 U.S.C. §101. Specifically, the examiner stated in the February 8, 2006, Office Action:

> 4. As to claims 1,19, Claims 1,19 are not limited to tangible embodiment, in view of Applicant's disclosure, specification page 2, lines 6-13, the computer program product is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., (microprocessor)) and intangible embodiment (e.g. (internet). Although applicant amended the program product residing on a computer readable medium for causing the execution, no practical application can be found in the clamed invention. The examiner understands the program product being stored in the computer readable medium to cause execution , but

> the focus is not on whether the steps taken to achieve a particular result is useful, tangible, concrete, but rather the final result is useful, tangible and concrete (page 20 of the internal guideline newly updated on 01/17/06). Claim 1 recites to cause execution, and it is read as a step taken to achieve practical result, but it is not a final result. Claim 1 also recites to branch to an instruction at a specific address at a value of availability of resource, but no substantial practical application can be found in the claim. As such, the claim is not useful, tangible and concrete, and is therefore non-statutory. (February 8, 2006, Office Action, page 3, Paragraph 4).

Applicant amended independent claim 1 and 19 to recite that the computer program product resides on a computer readable storage medium, to clarify that the subject matter of independent claims 1 and 19 is directed to tangible embodiments of the claimed computer program product (that is, computer program product stored on a computer-readable storage medium).

As for the examiner's contention that the subject-matter recited in these claims allegedly does not achieve a useful, tangible and concrete final result, applicant respectfully disagrees.

Applicant does not believe that the test is whether "the subject-matter recited achieves a useful, tangible and concrete final result." Rather, for computer program claims it is merely sufficient that the program be embodied on a concrete and tangible medium. Nevertheless, the computer program product of applicant's amended independent claims 1 and 19 includes a branch instruction that causes a data processing apparatus and/or processor to evaluate a branch condition relating to whether a state, of a state name indicating the availability of a resource, is a specified value, and to branch to a specified address based on that evaluation. The branch condition evaluation and the branching operation that may ensue are useful, tangible and concrete in that program flow control is achieved through the operations performed by the branch instruction. The branch evaluation and branching operations are also final results in that the sequence of operations recited in independent claims 1 and 19 achieve a final determination of how program flow of the currently executing instruction sequence of instruction stream is to proceed. Applicant thus traverses the examiner's rejections of independent claims 1 and 19 under 35 U.S.C. §101.

Applicant further notes that the language in the preamble of amended claims 1 and 19 conforms to the conventional form widely used to recite computer program product claims. Such claims are regularly used and appear in numerous issued patents including, for example, recently issued U.S. Patent Nos. 7,099,870, 6,961,787, 6,961,686, and 6,954,833.

The examiner maintained his rejections of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,724,563 to Hasegawa.

In addition, the examiner rejected claims 1 and 19 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,454,595 to Cage. Further, the examiner maintained his rejection of claims 1, 10 and 19 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,275,508 to Aggarwal, and also maintained his rejections of claim 1 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,640,538 to Dyer.

Specifically, with respect to applicant's claim 4 which, as noted, recited a feature similar to the feature added to amended independent claim 1, the examiner stated in the February 8, 2006, Office Action:

> 16. As to claim 4, Hasegawa also included microengines (see fig.9 instruction register 8, instruction decoder 3 and execution unit 11). (Office Action, page 6)

Additionally, with respect to claims 16 and 17, which recite microengines-related features that are similar to the features recited in amended independent claim 1, the examiner stated in the February 8, 2006, Office Action:

> 22. As to claims 16, Hasegawa also included a register stack (see fig.l (register file) and a arithmetic unit (not explicitly shown as ALU, but it showed arithmetic calculations in col.1, lines 20-25, col.7, lines 44-52, see the adder in col.7, lines 52-56, fig.1 , see counter section 4 in col.7, lines 8-26 for the increment and decrement, and comparison of the counter, see also the calculation section 7 in col.63-67, col.8, lines 1-4, and see also the arithmetic result flags in col.11 , lines 25-32). See also the branch on' over flow set and branch on overflow clear in Table 1 for the feature of evaluating the specified value.
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> 23. As to claim 17, Hasegawa did not explicitly show the additional microengine as claimed. However, Hasegawa , in the same patent, taught the parallel processor pipeline processor 200) could be implemented in two kinds of hardware having respective different instructions set for use the same program code for both hardware

(see col.13, lines 7-12). Therefore, additional hardware (or microengine) was applicable in Hasegawa. (Office Action, pages 7-8)

Applicant's independent claim 1 recites "cause an executing instruction stream to branch to an instruction at a specified address if a state, of a state name specified in the branch instruction is a specified value, with the state indicating the availability of a resource of the data processing apparatus, wherein the state is available to a plurality of microengines, each of the plurality microengines having control logic and an execution box, the execution box including an arithmetic logic unit and a general purpose register set, each of the plurality of microengines being configured to process a plurality of threads." Thus, a decision to branch to a specified address depends on the availability of a resource of the data processing apparatus, as identified by a state name that is specified in the branch instruction being executed. The state upon which a branch decision is made is made available to a plurality of microengines so that erroneous branch decisions could be avoided by enabling the microengines to have access to the current state value.

In contrast Hasegawa discloses a pipeline processor that can execute predictive branch instructions (Abstract). While Hasegawa's processor includes a register file 12 and an execution section 11, at no point does Hasegawa disclose that a plurality of such processors are used, each of which being configured to process a plurality of threads. In fact, nowhere is it disclosed that Hasegawa's processor is capable of executing anything more than just a single process. Because Hasegawa's architecture does not include a plurality of microengines, Hasegawa's processor cannot make a state, indicating the availability of a resource, available to a plurality of microengines. Accordingly, contrary to the examiner's contention, Hasewaga does not disclose or suggest at least "cause an executing instruction stream to branch to an instruction at a specified address if a state, of a state name specified in the branch instruction is a specified value, with the state indicating the availability of a resource of the data processing apparatus, wherein the state is available to a plurality of microengines, each of the plurality microengines having control logic and an execution box, the execution box including an arithmetic logic unit and a general purpose register set, each of the plurality of microengines being configured to process a plurality of threads," as required by applicant's independent claim 1.

The examiner contended that Hasewaga col. 13, lines 7-12, discloses the use of additional microengines in Hasewaga's apparatus. The above-identified excerpt from Hasewaga describes:

> **In addition, in the case where the pipeline processor 100 is implemented in two kinds of hardware having respectively different instruction fetch cycle numbers, it is possible to use one and the same program code for both kinds of hardware, which also ensures a continuous use of a program code which was produced in the past.**

All the above-quoted paragraph discusses is that in the event that a different hardware implementation is used for the processor described in Hasewaga, the same type of predictive branch instruction code that was designed to operate on the first hardware implementation could also operate on the other hardware implementation. Nowhere in that passage or Hasewaga generally is it suggested that both hardware implementations would be integrated into a single processor, and be capable of operating in concert. Accordingly, Hasewaga does not disclose or suggest operability of multiple processors (or microengines).

Applicant's independent claim 1 is thus patentable over the cited prior art.

Claims 2-3, 5, 7-9 and 21-22 depend from independent claim 1 and are therefore patentable for at least the same reasons as independent claim 1.

Independent claims 10, 16 and 19 recite "evaluating a value of a state name specified in a branch instruction, the value of the state name indicating the availability of a resource of the processor; and performing a branching operation based on the value of the specified state name being set or cleared, wherein the state is available to the multiple microengines, each of the multiple microengines having control logic and an execution box, the execution box including an arithmetic logic unit and a general purpose register set, each of the plurality of microengines being configured to process a plurality of threads," or similar language. At least these features are not disclosed by the prior art cited by the examiner for reasons similar to those provided with respect to independent claim 1. Accordingly, independent claims 10, 16, and 19 are patentable over the prior art.

Claims 11-15 depend from independent claim 10 and are therefore patentable for at least the same reasons as independent claim 10. Claims 17-18 depend from independent claim 16 and are therefore patentable for at least the same reasons as independent claim 16. Claim 20 depends

from independent claim 19 and is therefore patentable for at least the same reasons as independent claim 19.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply charges or credits to deposit account 06-1050, referencing attorney docket 10559-306US1.

Respectfully submitted,

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